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High Resolution Electronic Measurements in Nano-Bio Science

ANALOG VS DIGITAL LOCK-IN PROCESSING

Francesco Zanetto

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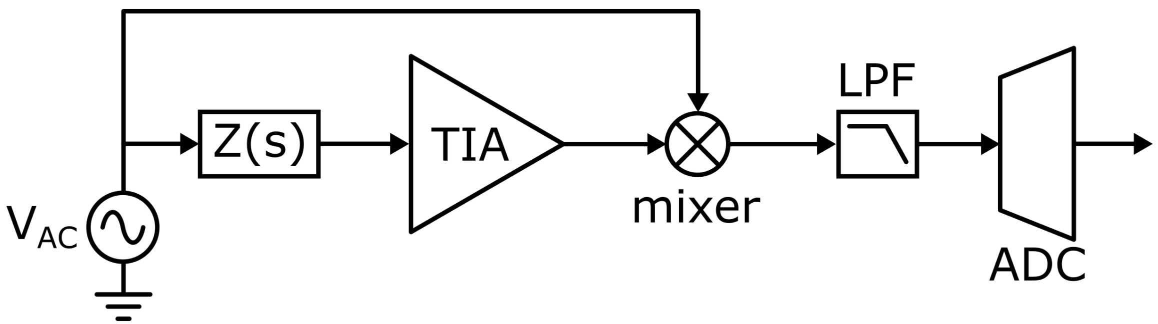
Analog vs digital lock-in processing

- Lock-in amplifiers are commonly divided into analog and digital instruments.
- Both classes of instruments require ADCs and DACs to be implemented, the difference stands in how the demodulation process is carried out.
- Analog LIAs perform the demodulation in the analog domain and digitize the low frequency output of the mixer.
- Digital LIAs digitize the high frequency signal and then demodulate it in the digital domain.



ANALOG LIA

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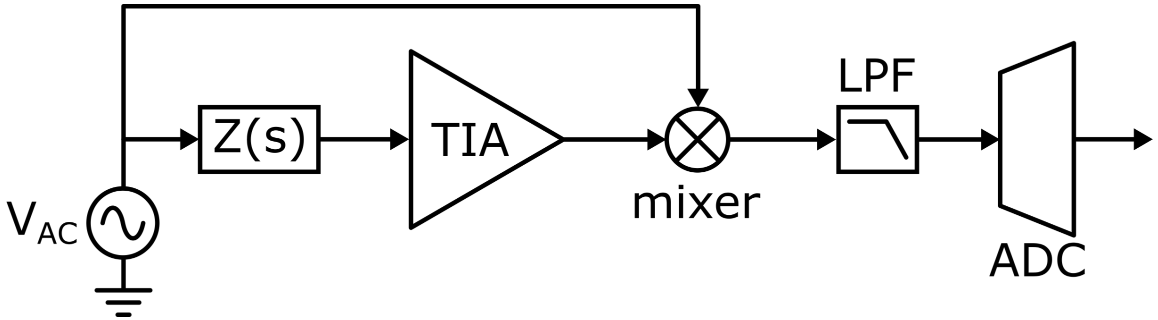
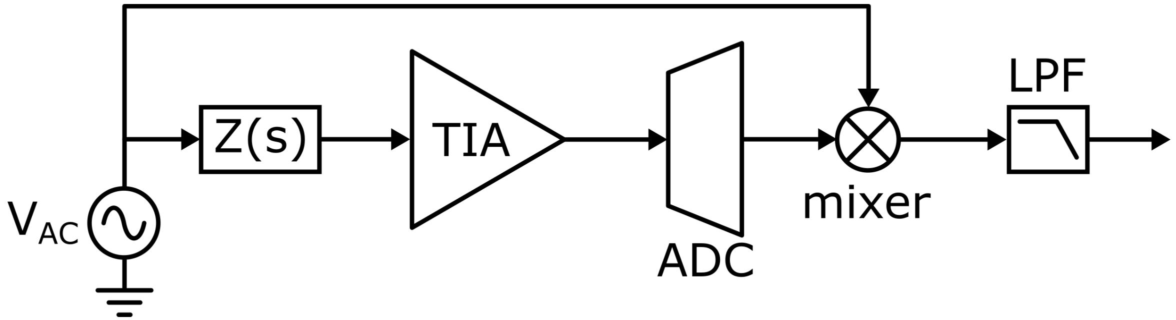


<u>ANALOG LIA</u>



<u>DIGITAL LIA</u>

Pro & cons of analog and digital lock-in amplifiers

Analog

PROS

- By changing only the front-end amplifier and mixer, any stimulation frequency can be used.
- It does not require fast ADCs and digital signal processing.
- Simple implementation even in integrated circuits.

CONS

- Sensitive to 1/f noise of any stage after the demodulation (mixer, further gain stages, …)

Digital

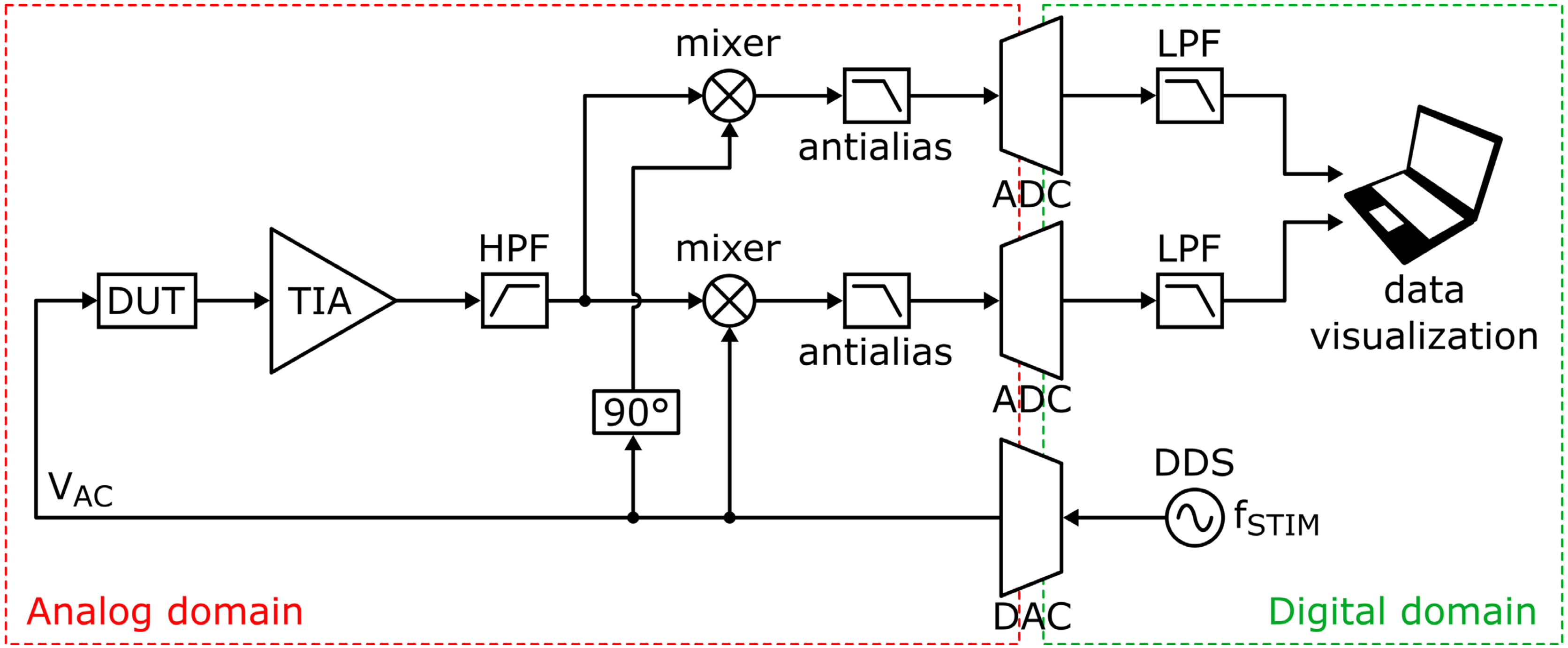
PROS

- Insensitive to 1/f noise of its building blocks.
- It can achieve sub-ppm resolution.
- Less components are required.

CONS

- Fast ADCs and complex digital signal processing are required.
- Implementation in ICs is not trivial, especially for high stimulation frequencies.

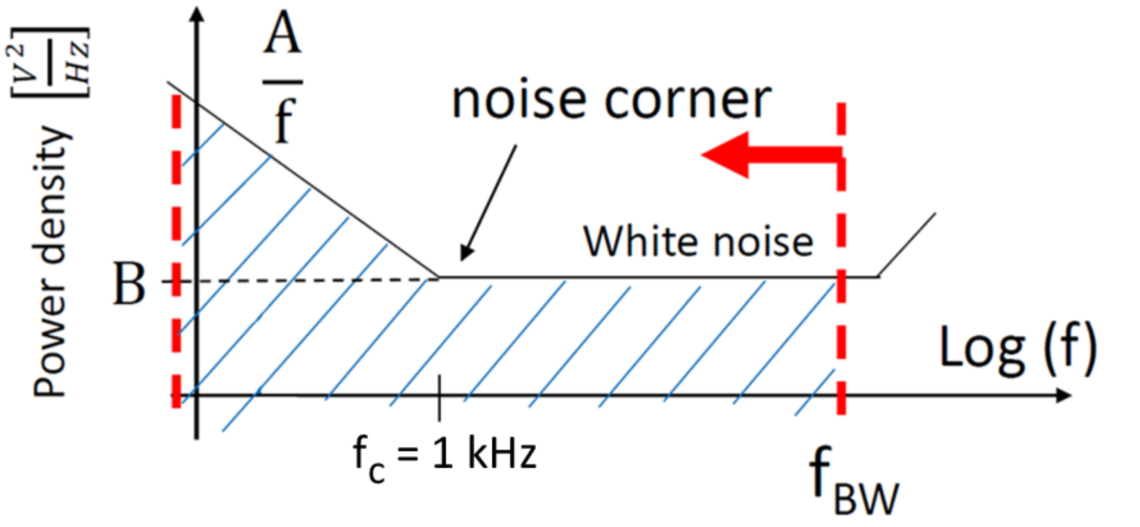
Analog lock-in structure



- An (optional) high-pass filter can be used to remove the DC component before the demodulation.
- Two acquisition chains are needed after the TIA to perform I/Q demodulation and fully reconstruct the DUT impedance.
- A low-pass filter is used to avoid aliasing effects in the ADC acquisition, further low-pass filtering can be done digitally to reduce the readout bandwidth if needed.

Requisite for using analog lock-in amplifiers

- The analog lock-in amplifier has the same noise performance as the digital one if the readout bandwidth is sufficiently larger than the 1/f noise corner frequency of the overall circuit.
- This ensures that the 1/f contribution is negligible with respect to the white noise.
- <u>As a rule of thumb, the readout bandwidth should be roughly 10 times larger than the 1/f noise corner frequency.</u>



$A = 100 \cdot 10^{-15}\ [V^2]$ $\quad \sqrt{B} = 10\ nV/\sqrt{Hz}$

$f_C = 1\ kHz$

1/f white

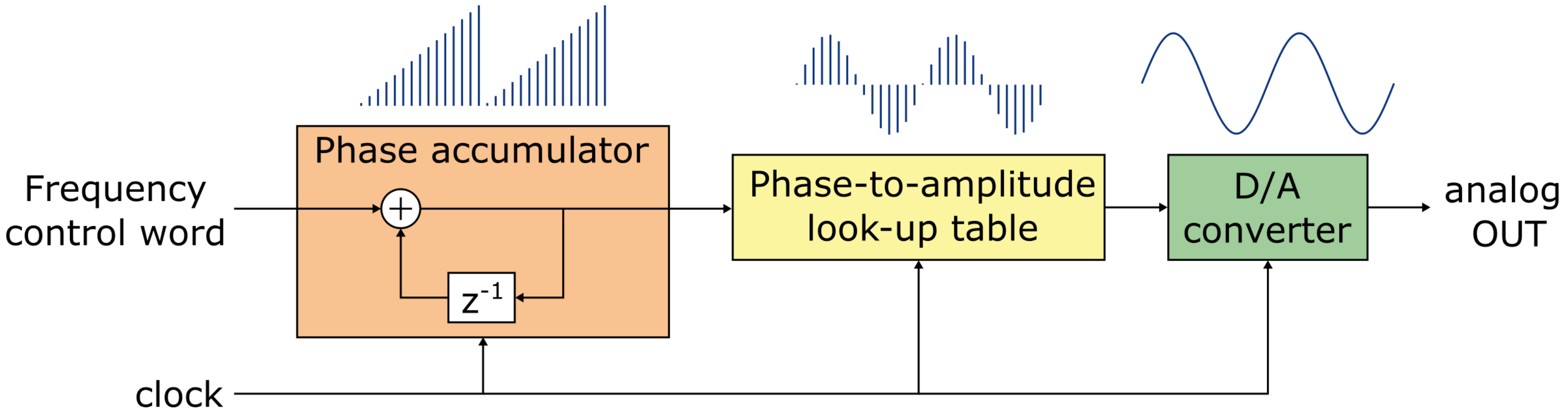
$$f_{BW} = 1\ MHz \rightarrow v_{N,RMS}^2 = 1.6 \cdot 10^{-12} + 10^{-10}\ [V^2]$$

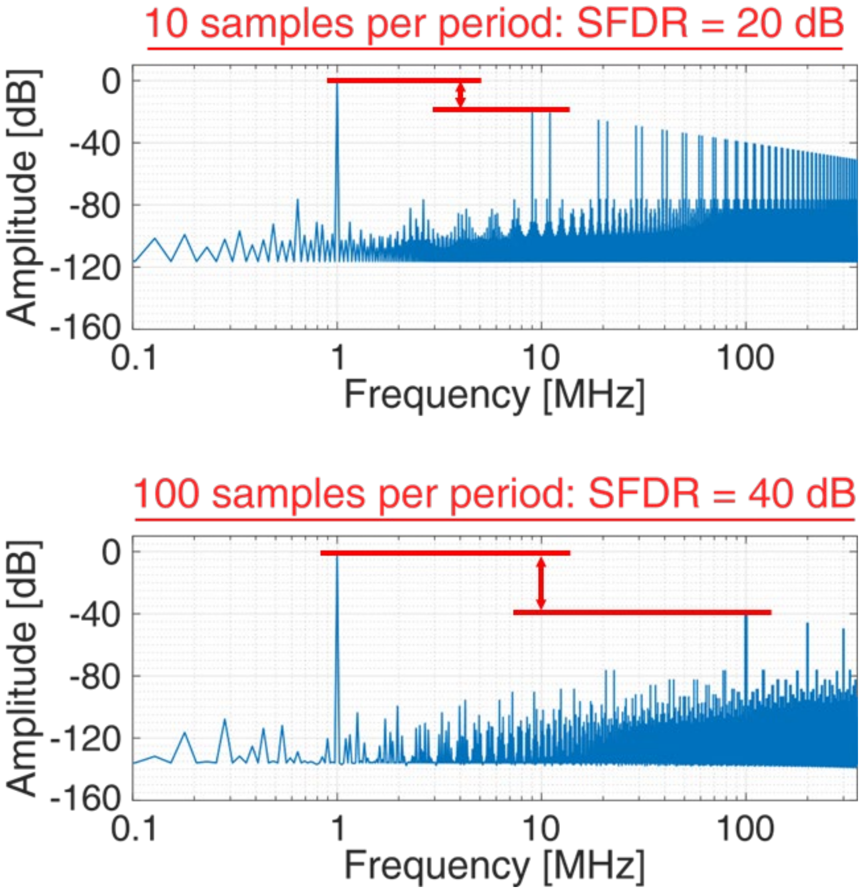
$$f_{BW} = 100\ kHz \rightarrow v_{N,RMS}^2 = 1.38 \cdot 10^{-12} + 10^{-11}\ [V^2]$$

$$f_{BW} = 10\ kHz \rightarrow v_{N,RMS}^2 = 1.15 \cdot 10^{-12} + 10^{-12}\ [V^2]$$

Generation of the lock-in signals

- The stimulation chain can be a source of noise in the measurement. Make sure to choose the right components not to worsen the lock-in performance.
- The stimulation and I/Q demodulation signals are usually generated with a direct digital synthesizer (DDS).





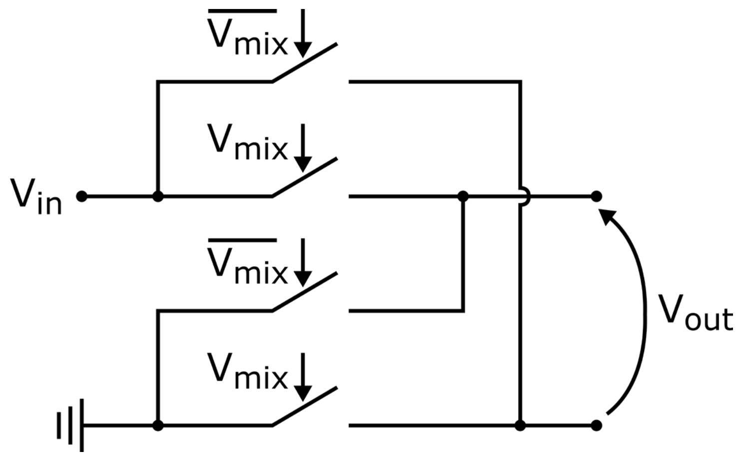
Increasing the number of samples per sinusoid period improves the spectral purity of the stimulation signal and allows to better filter out the spurious harmonics.

Mixer

- The mixer is critical in setting the lock-in amplifier performance because any non-ideality is directly translated into a measurement error.
- It should have output offset and 1/f noise as low as possible and sufficiently high bandwidth and linearity (in the case of sinusoidal multipliers).

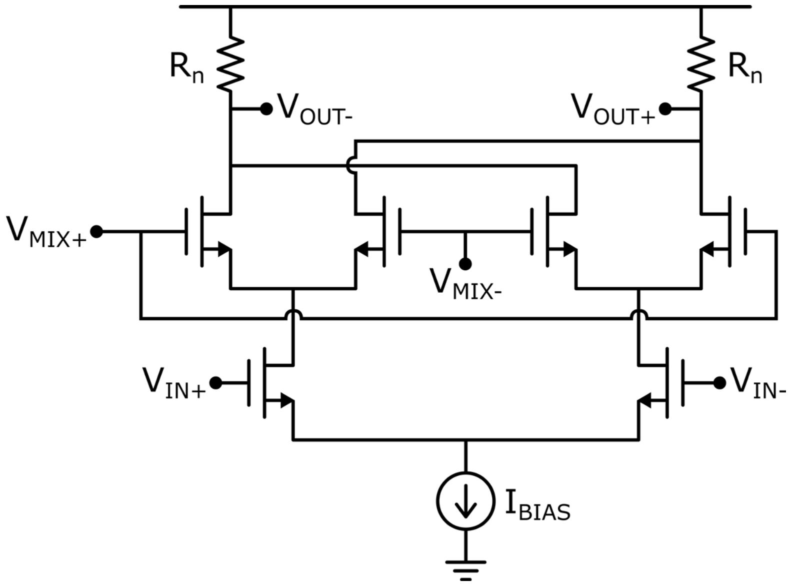
Passive mixer

- Low 1/f noise, only square wave demodulation



Active mixer

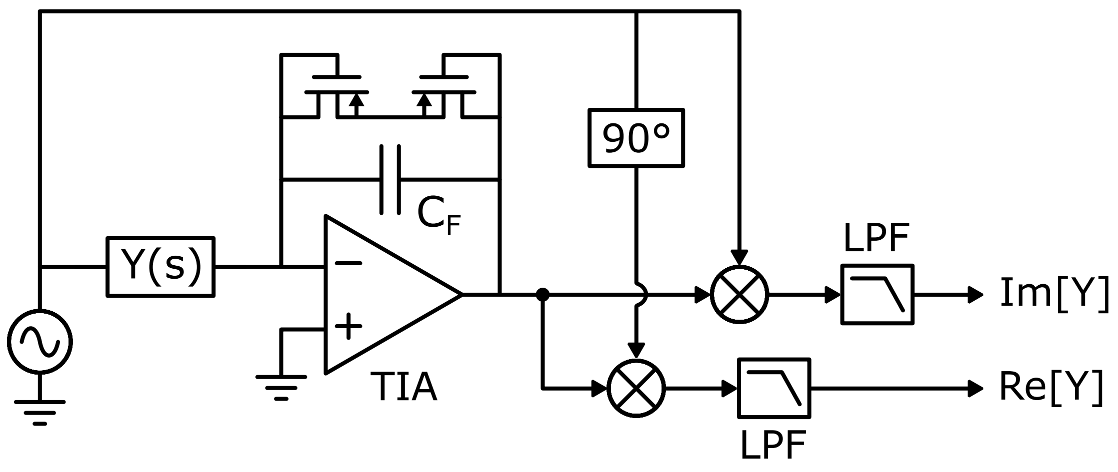
- Higher 1/f noise, more complex but sinusoidal demodulation possible.



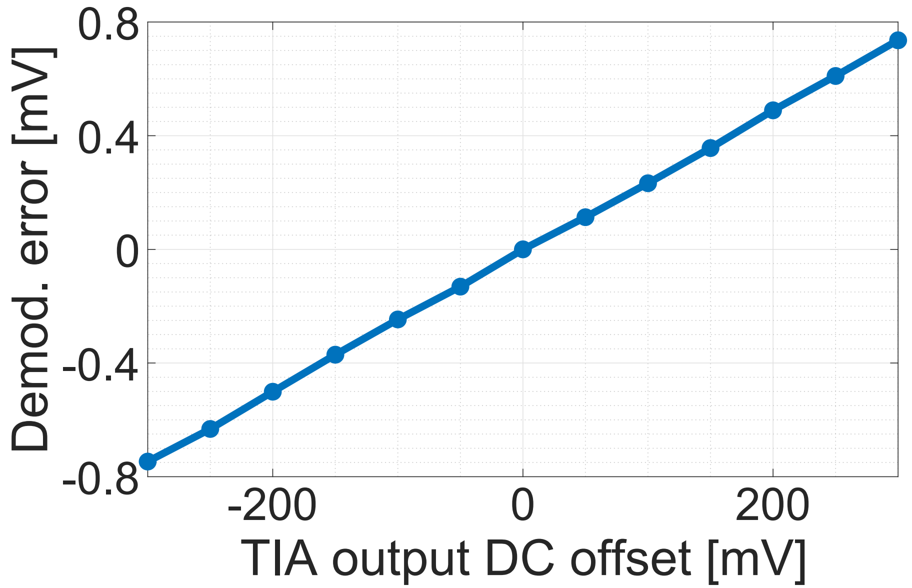
Mixer non-idealities

- Measurement errors introduced by the mixer cannot be removed because the signal has already been moved to low frequency.
- Try to make the mixer work always in the same operating conditions (for example, remove DC offset before the demodulation) to avoid signal-dependent errors.

Example: DC offset at mixer input can translate into demodulation error

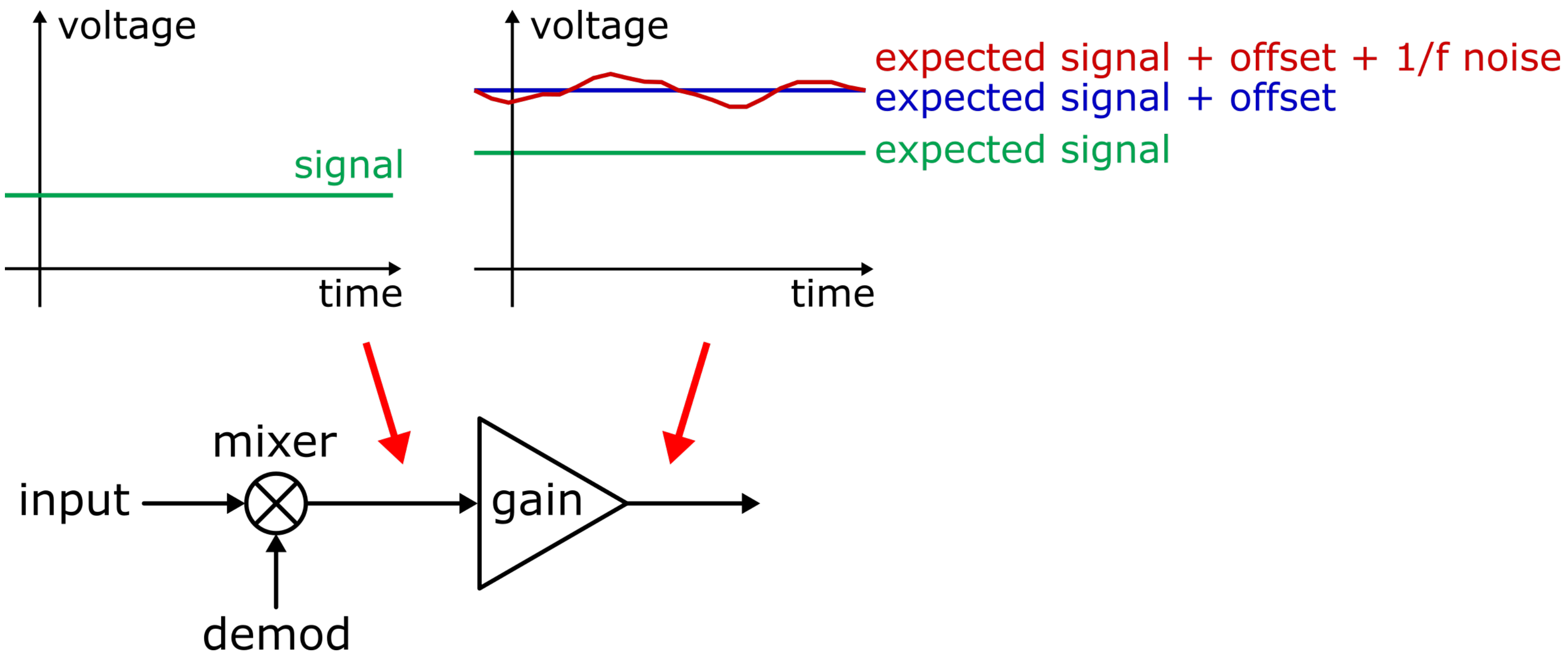


No HPF before mixer



Amplification after the mixer

- If further amplification is needed after the mixer, choose an amplifier with very low 1/f noise corner frequency and offset, because they are summed directly to the signal to be measured and can't be removed afterwards.
- Chopper-stabilized amplifiers are a good option, because they are specifically designed for these applications.



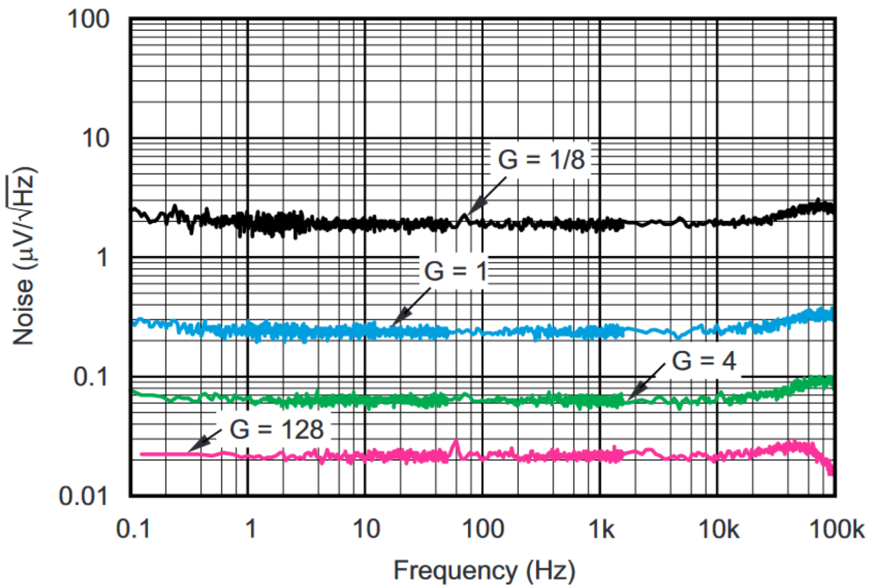
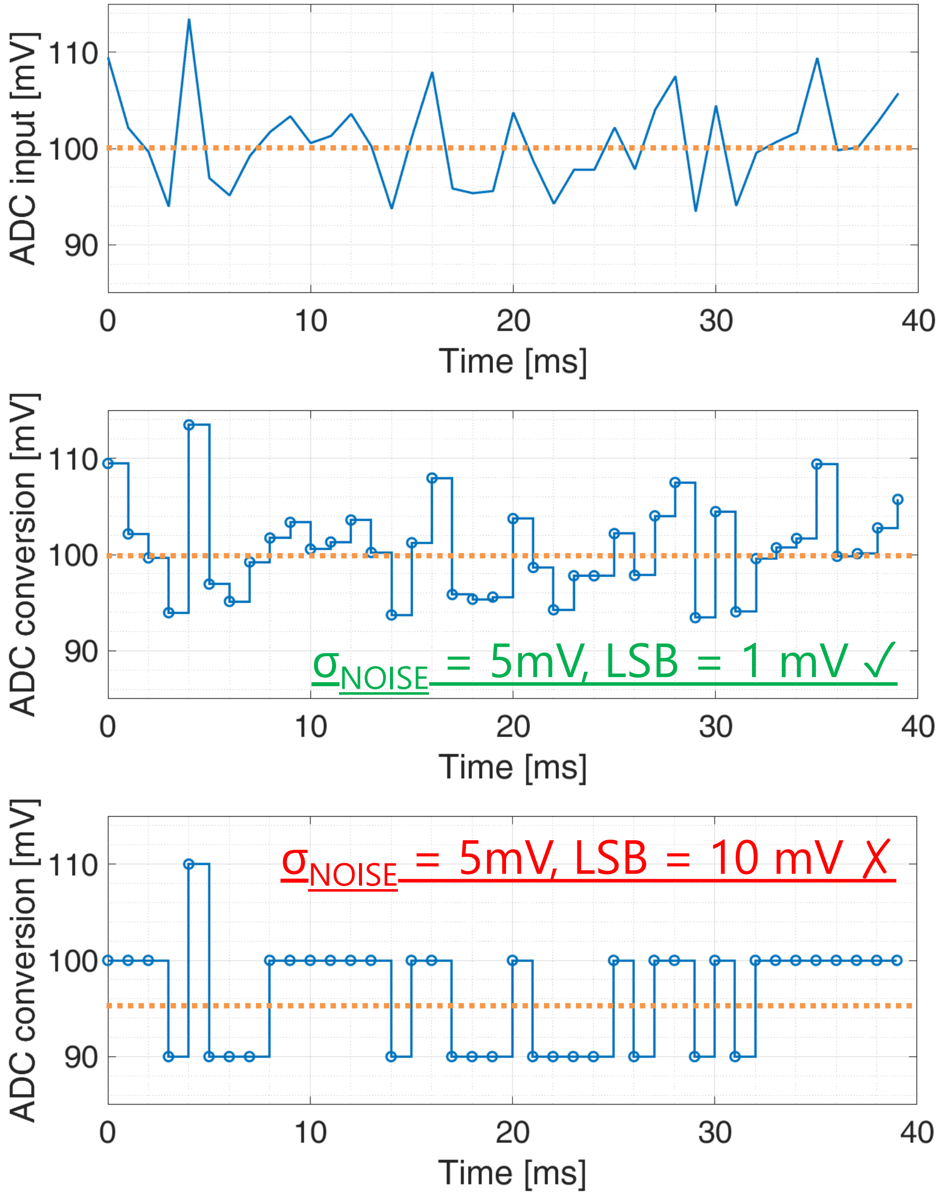


Figure 15. INPUT-REFERRED NOISE SPECTRUM

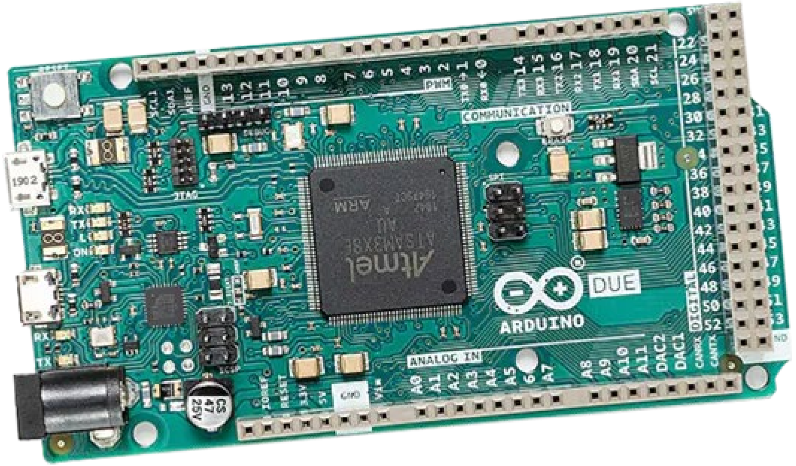
Analog to digital conversion

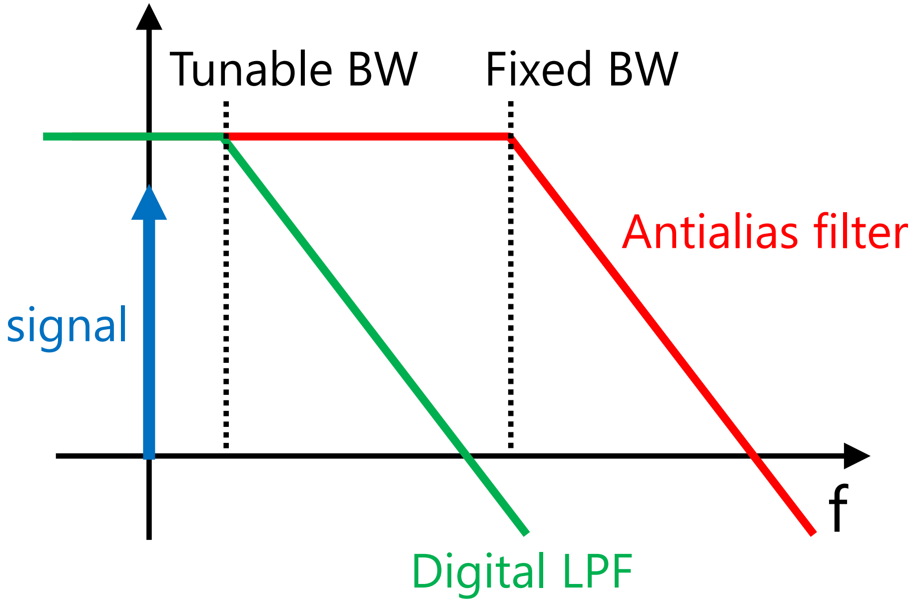
- A slow ADC is enough to digitize and acquire the lock-in output, that is already a DC signal.
- Choose the ADC number of bits such that the LSB is much smaller than the RMS noise at the input of the converter.
- This guarantees that the measurement result is not affected by the A/D conversion.
- Oversampling (choosing $f_{SAMP} \gg BW_{READOUT}$) can be used to make the effect of the ADC quantization noise negligible on the measurement result.



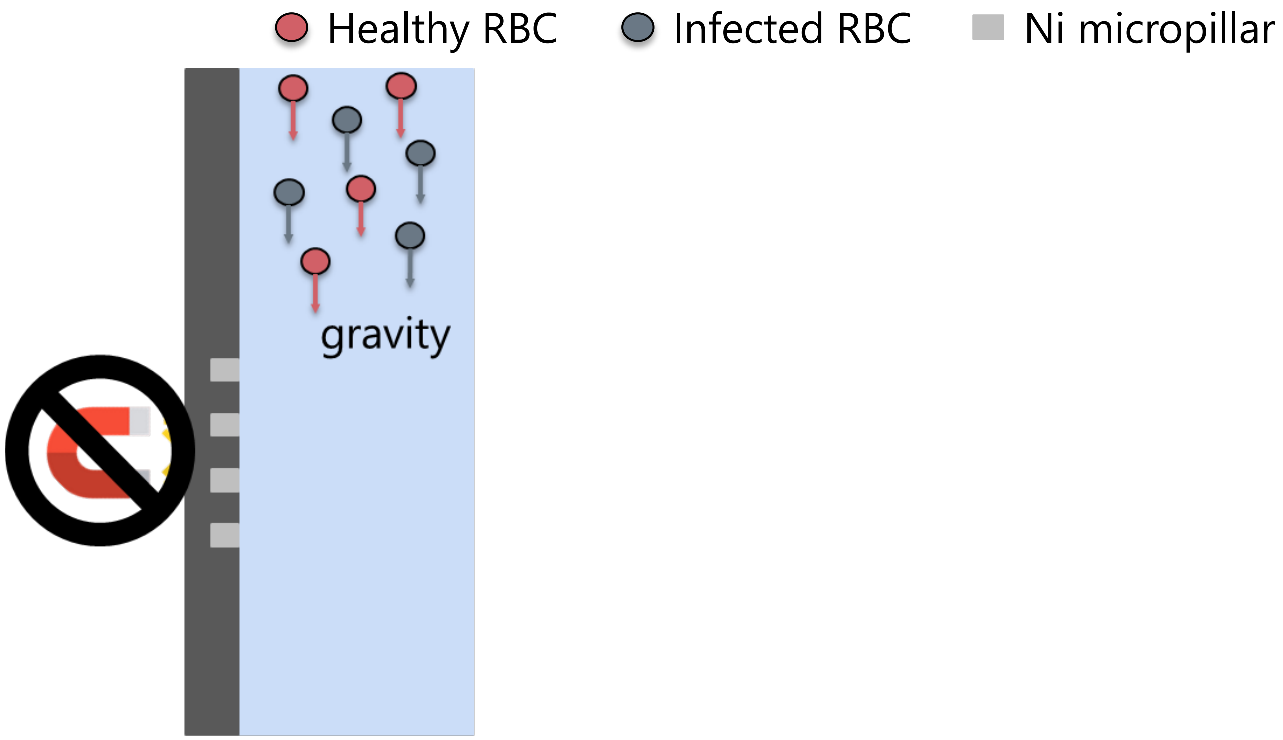
Digital signal processing

- A digital processor is used to control the ADC operations, acquire the conversion result and provide it to the user.
- Usually a standard microcontroller (Arduino, STM32, …) is enough to perform this tasks since all the operations are performed at low speed (tens of kHz).
- A digital low-pass filter (such as a moving average filter) can be implemented on the microcontroller to further reduce the readout bandwidth and increase the measurement accuracy if needed.





- The malaria parasite infects red blood cells (RBC) and makes them magnetic by producing hemozoin crystals.
- This property can be used to develop a system-on-chip for malaria detection.
- Healthy cells sediment on the bottom of the chip while infected ones are captured with a magnet.
- The infected cells are detected by using impedance sensing electrodes.



M. Giacometti et al., IEEE TBIOCAS, vol. 16, no. 6, pp. 1325-1336 (2022)

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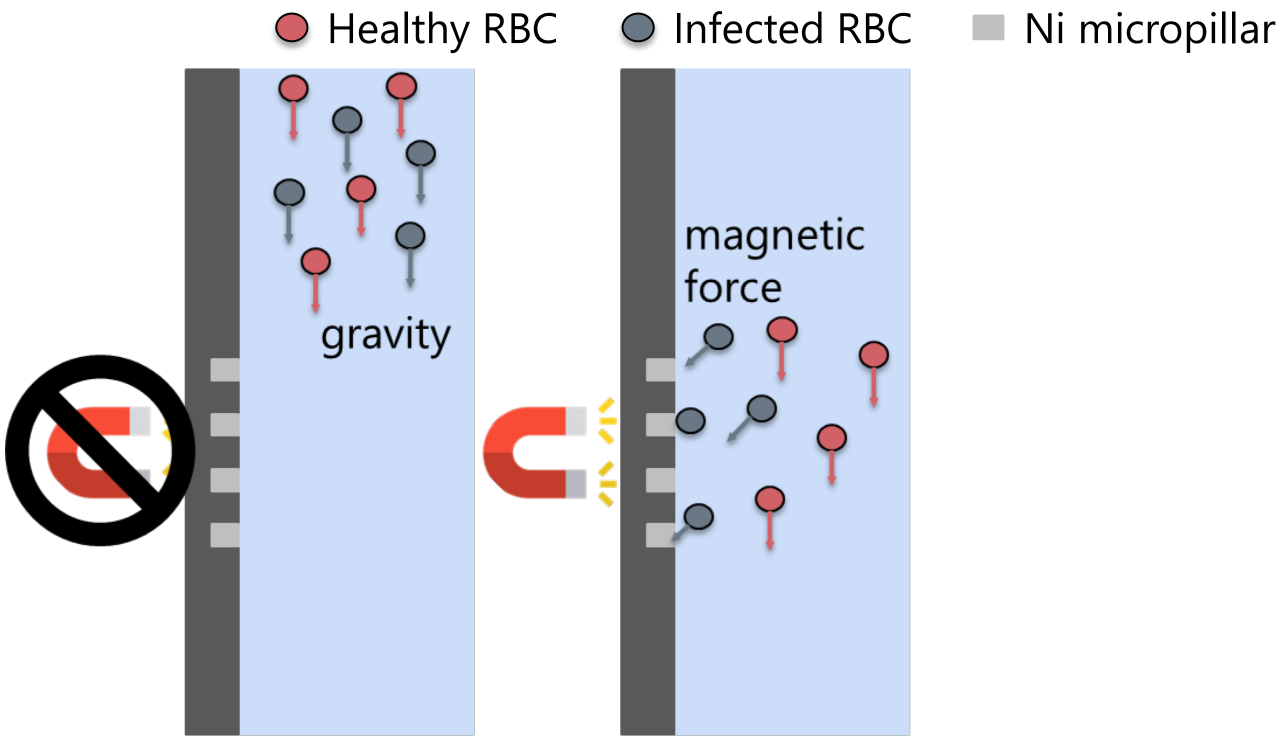

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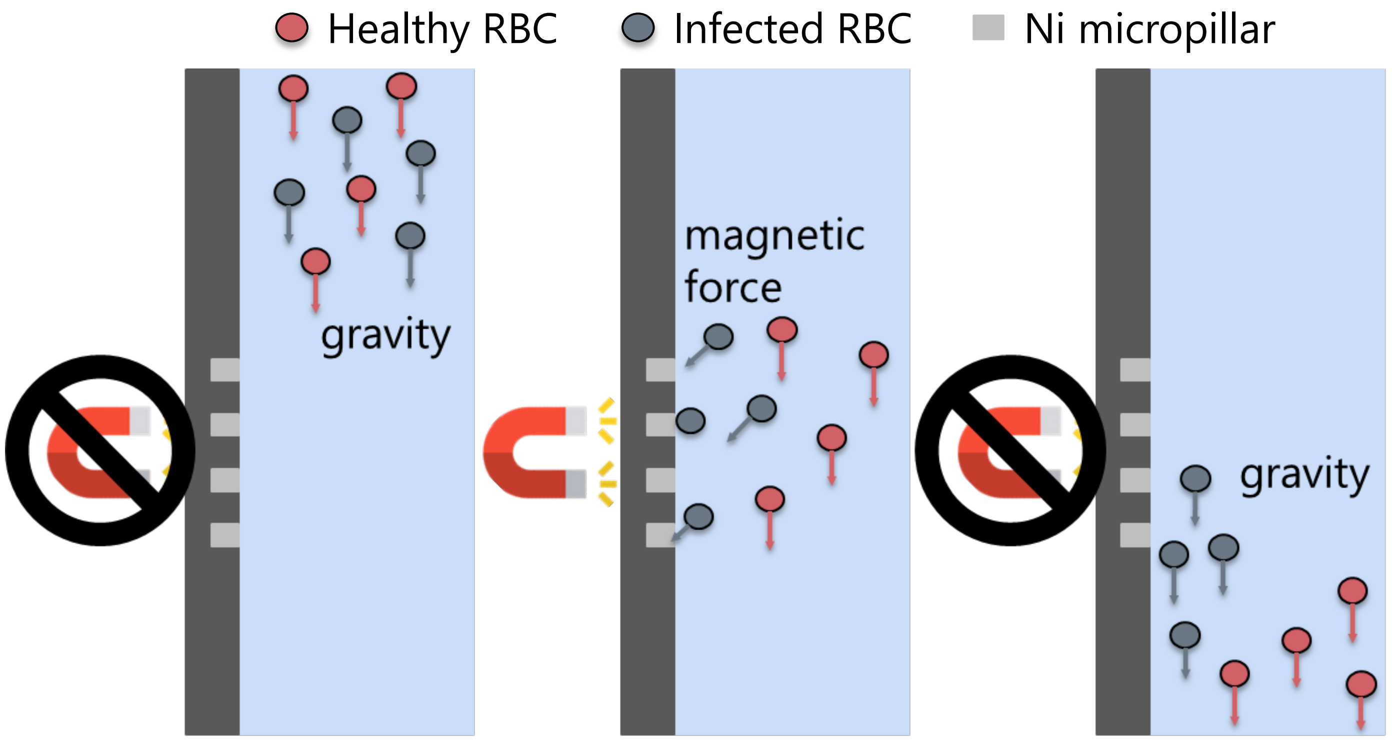

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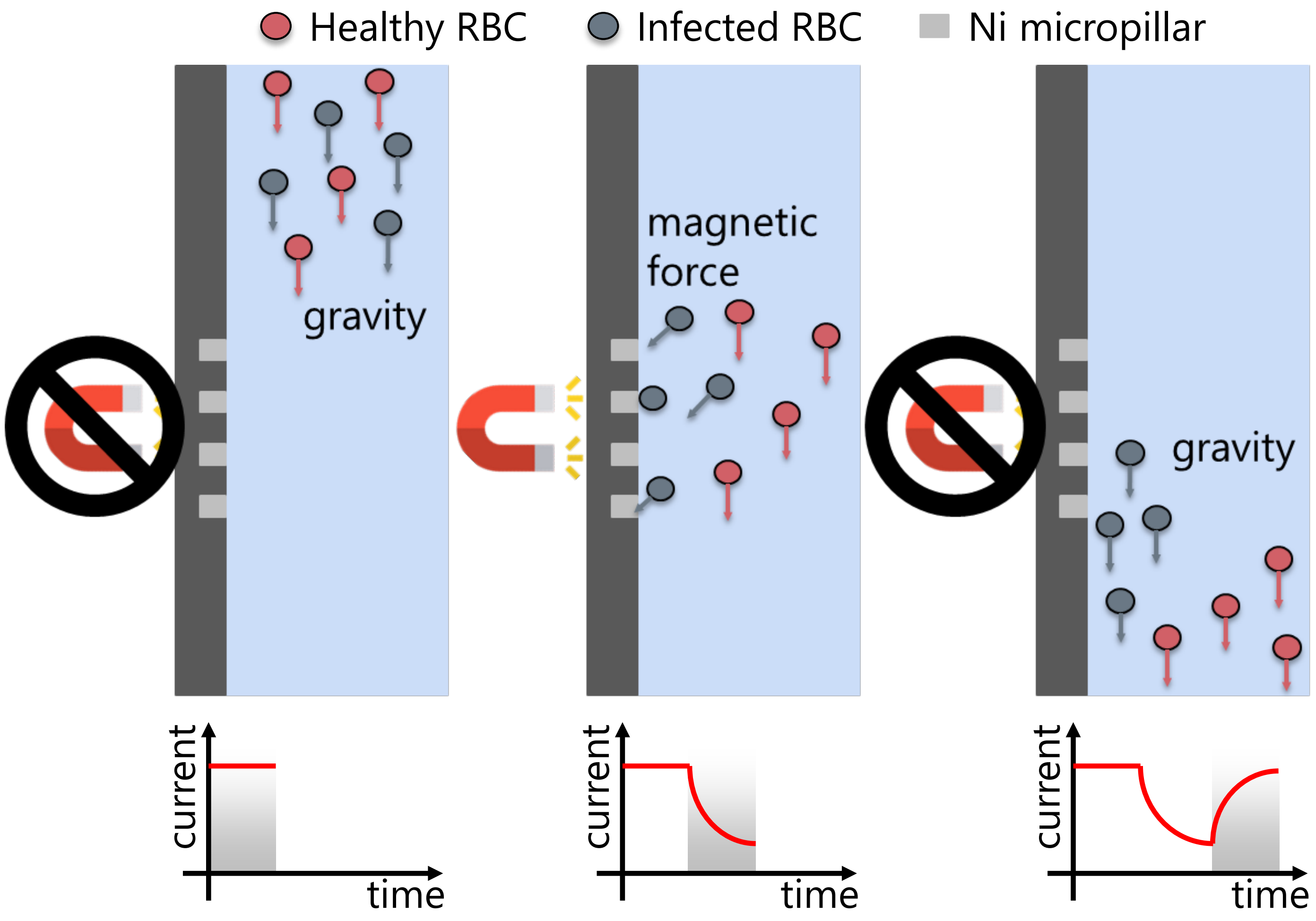

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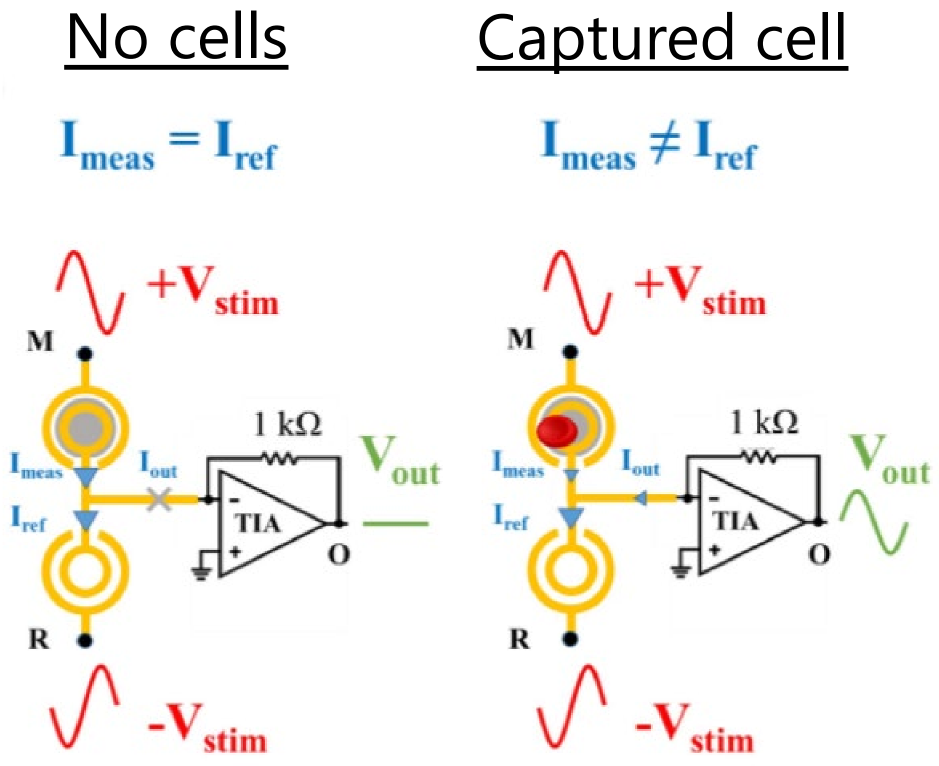
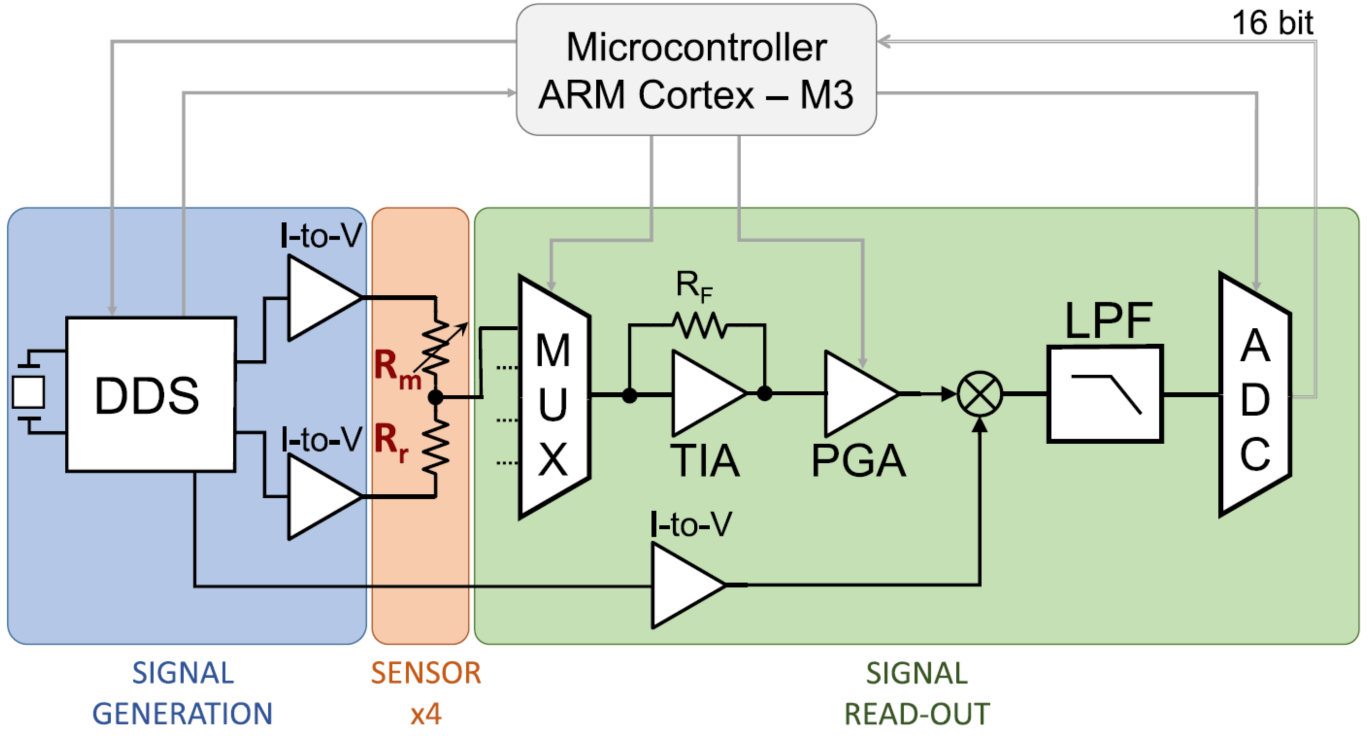


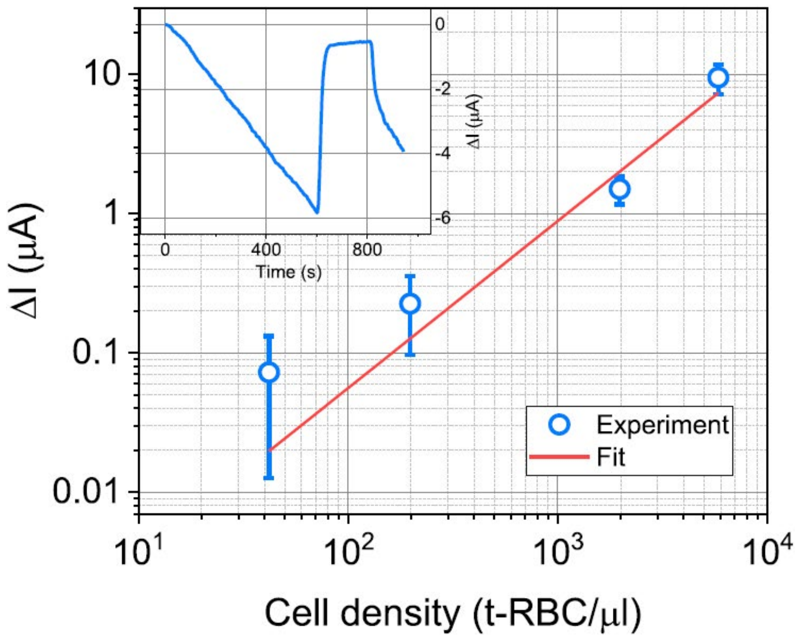
Differential electrodes to limit the effect of temperature fluctuations of the liquid.



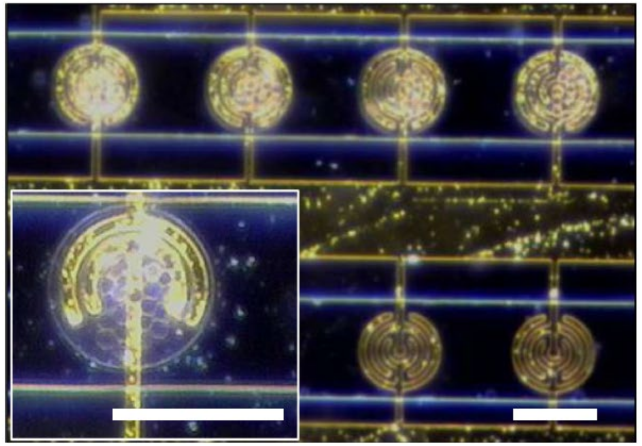
- The measurement accuracy is limited by the conductivity fluctuations of the liquid.

⬇

- A low-cost analog lock-in amplifier can be used to perform the impedance measurement at 1 MHz.



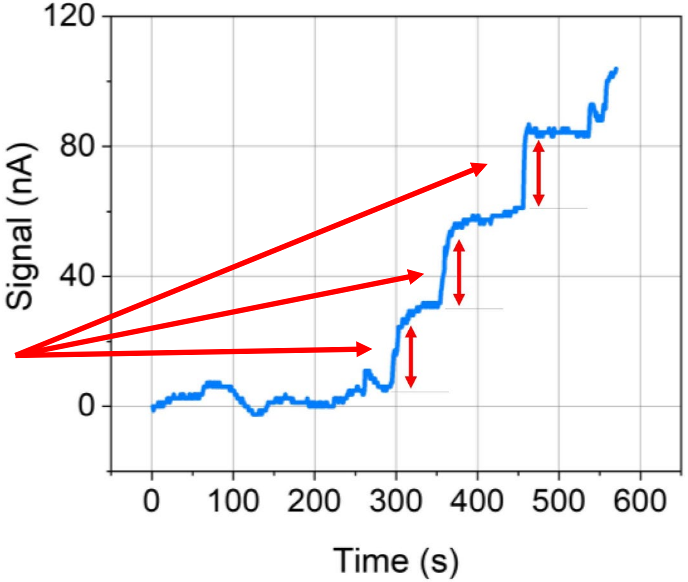
- Custom biochip with 91 differential electrodes in parallel for large sensing area.
- Successful detection down to 40 infected cells per μL of buffer solution.
- By optimizing the biochip layout, single cell detection can also be achieved at the price of a smaller sensing area.



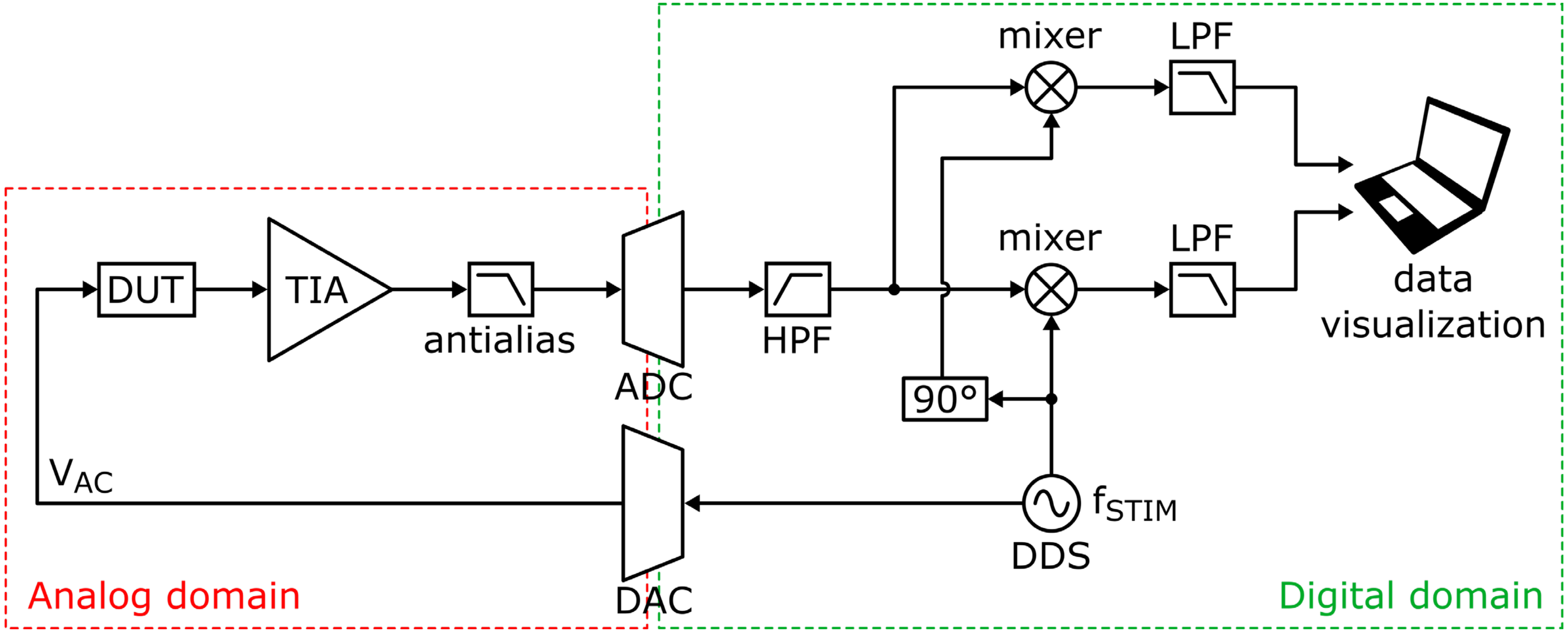
Active sensors

Reference sensors

Single cell capture



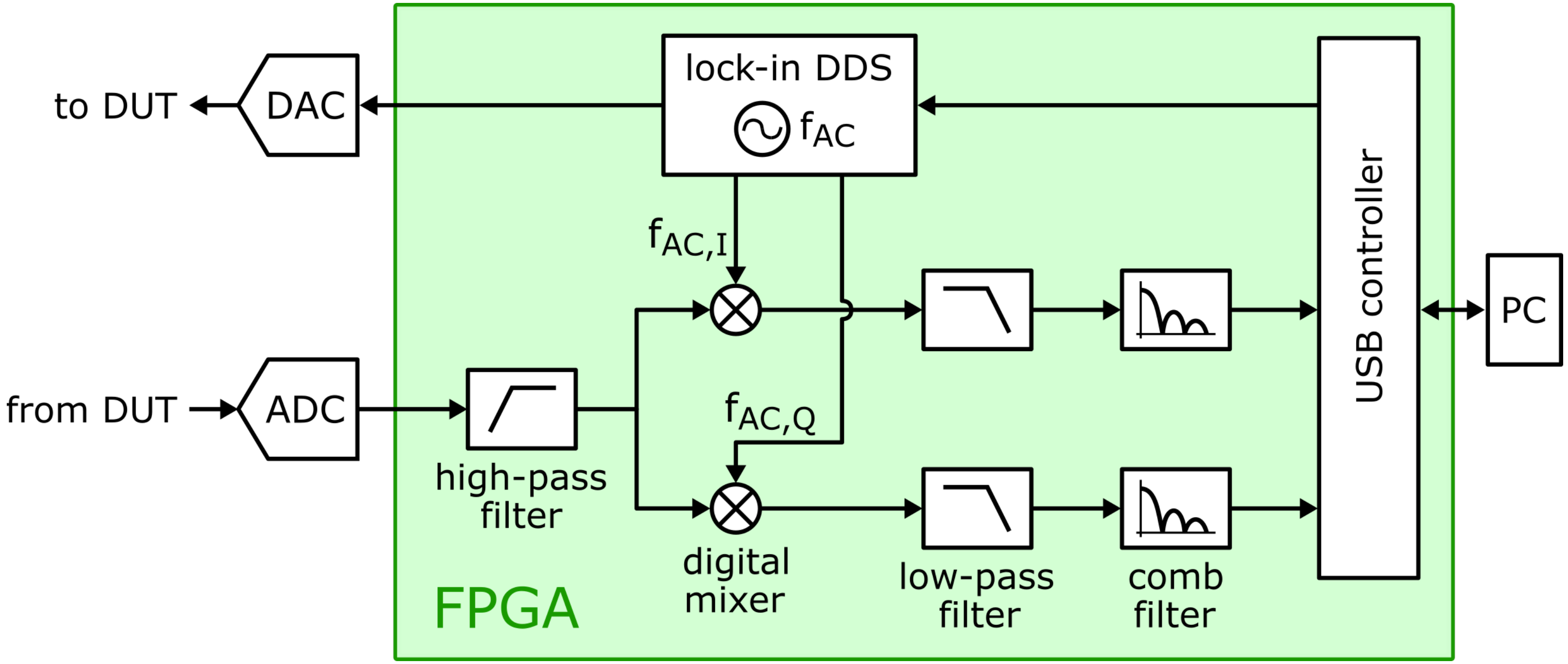
Digital lock-in structure



- The front-end circuit is the same as in an analog LIA, but a fast ADC is now required to correctly sample the high-frequency input signal.
- A single acquisition chain is needed, the I/Q processing is performed only in the digital domain → advantage in terms of area with respect to analog LIA.
- The 1/f noise and offset of the acquisition chain do not affect the measurement because the down-conversion is performed in the digital domain.

Digital signal processing (DSP)

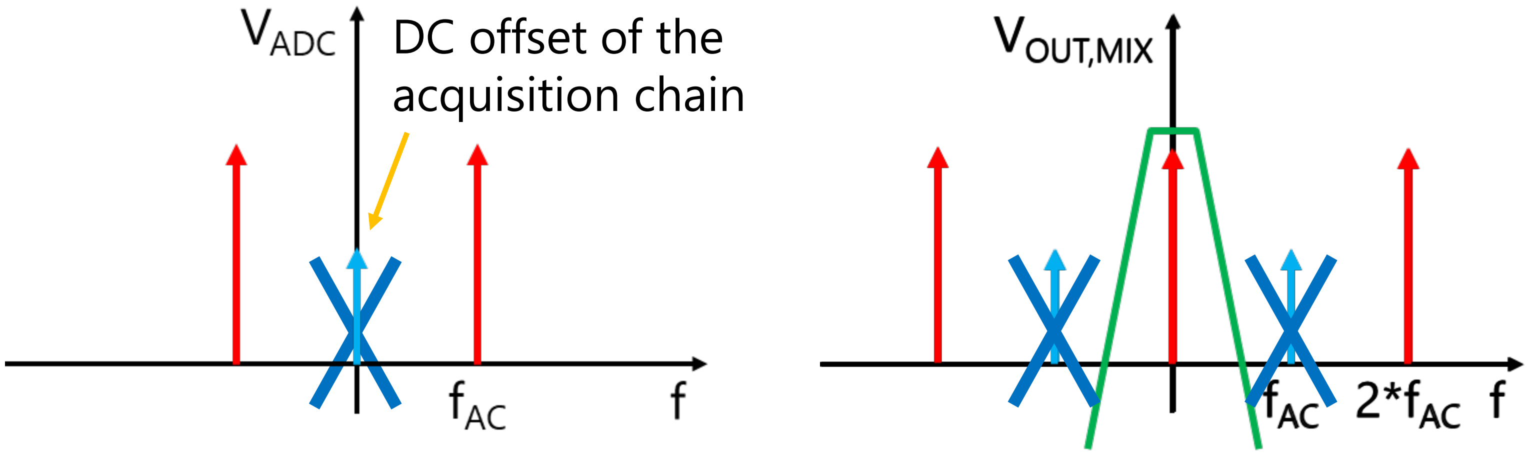
- A digital processor is needed to demodulate and filter the ADC readout.
- Especially when the lock-in is operated at high frequencies (tens of MHz), a microcontroller is not enough to perform real-time digital processing → FPGA-based digital LIAs are the most common approach.
- The DSP chain operates at the same frequency as the ADC sampling → for practical limitations of most FPGAs, it's hard to work at sampling rates above 100 MHz.



Suppression of the demodulation harmonics

The low-pass filter after the digital mixer has two main functions:

- Define the lock-in readout bandwidth.
- Suppress the harmonics generated by the demodulation process below the RMS noise level of the acquisition chain.



- Depending on the stimulation frequency and required readout bandwidth, the LPF can have challenging specifications in terms of out-of-band attenuation.
- A HPF before the mixer slightly the relaxes the LPF specs by removing the DC offset before it gets upconverted to f_{AC} by the mixer.

LPF requirements

<u>Example:</u>

V_{IN} = 2V_{pp} , $V_{noise,RMS}$ = 10 μV → required LPF attenuation: ≫50000

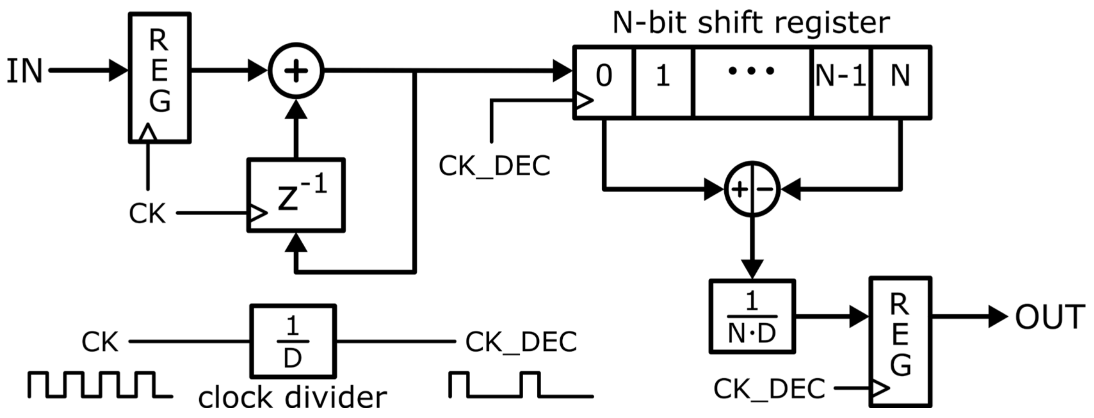
f_{AC} = 100 kHz, BW = 1 kHz → a first-order LPF provides an attenuation of only 200

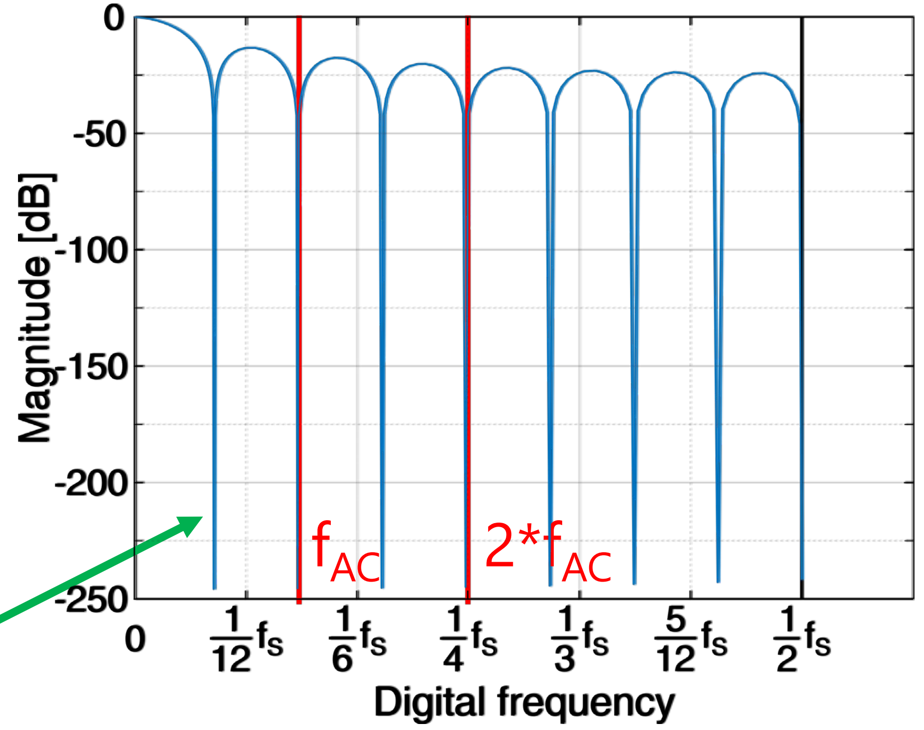
- <u>Complex high-order filters, requiring multiple digital adders and multipliers, are usually needed to completely suppress the high-order harmonics.</u>
- In real implementations, this is not always possible because of the limited hardware resources of standard FPGAs.

<u>Is there a better way to remove the harmonics by taking advantage of the fact that we know their frequency a priori?</u>

Cascaded integrator-comb filter

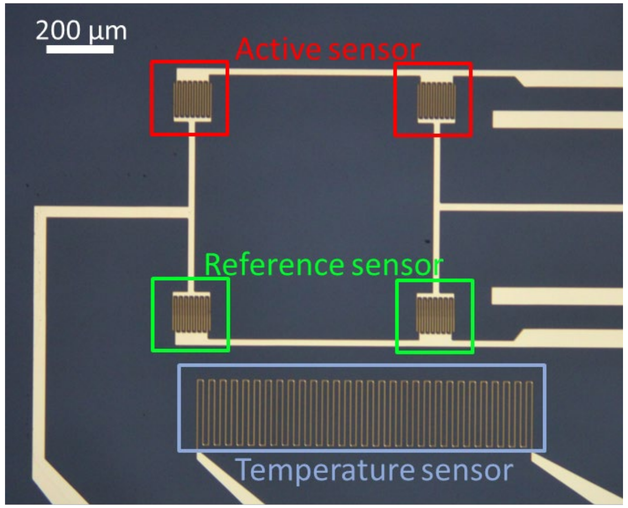
- A cascaded integrator-comb filter is an efficient hardware implementation of the moving average filter.
- It is characterized by notches in its transfer function, that can be set by the user by properly designing the filter structure.
- The notches can be conveniently positioned to completely suppress the demodulation harmonics without requiring many hardware resources.
- A first-order standard LPF can then be used just to define the readout bandwidth.

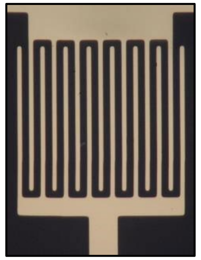


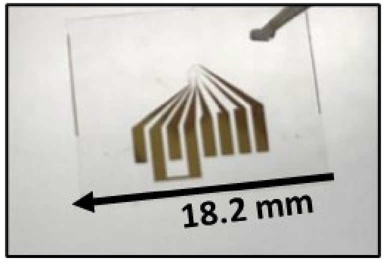


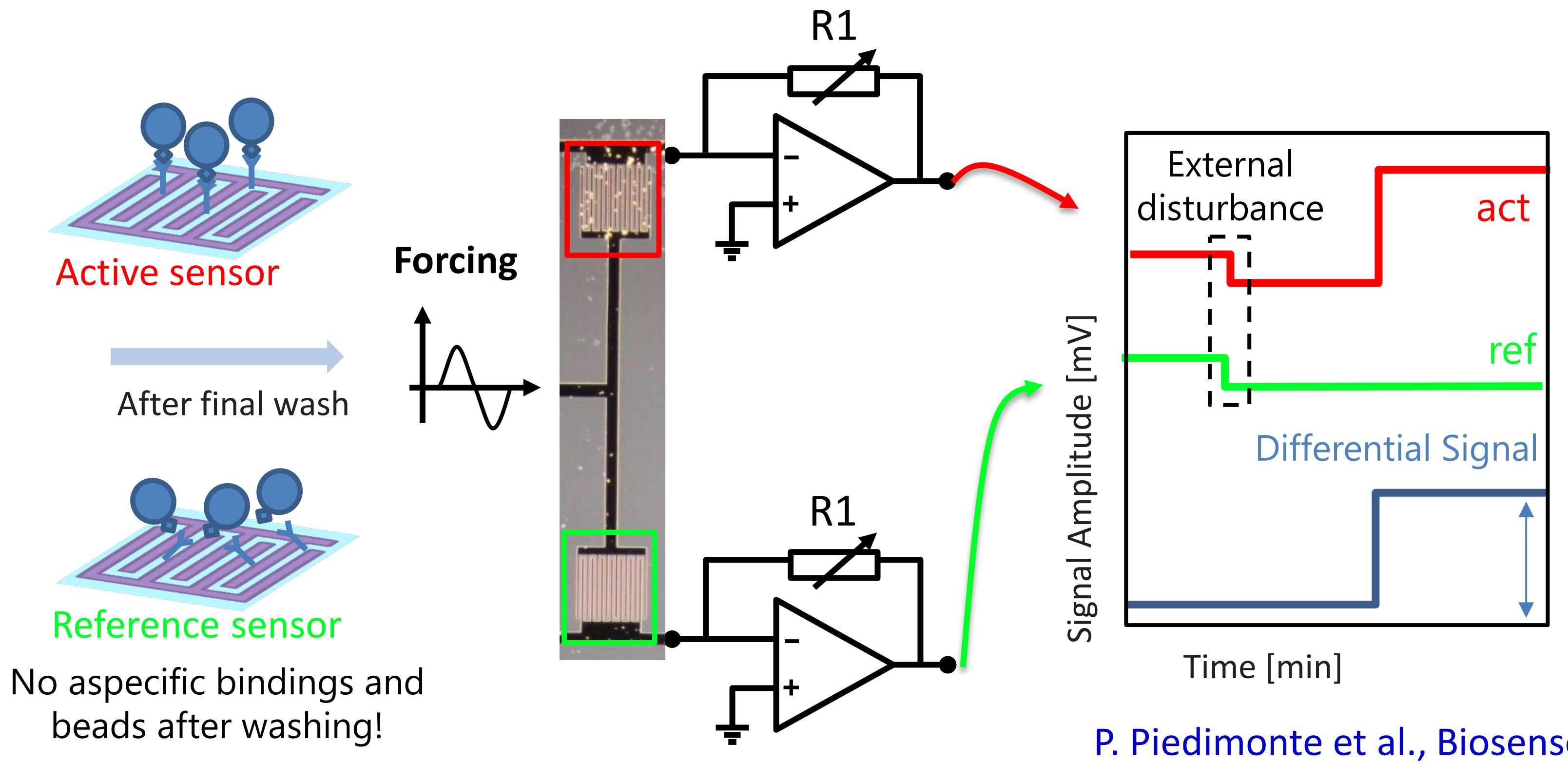
$f_{NOTCH} = f_S/N*D$

- Lab-on-chip with functionalized electrodes for simultaneous detection of multiple DNA targets.
- Differential measurement for rejection of all common mode signals by using non-functionalized electrodes.



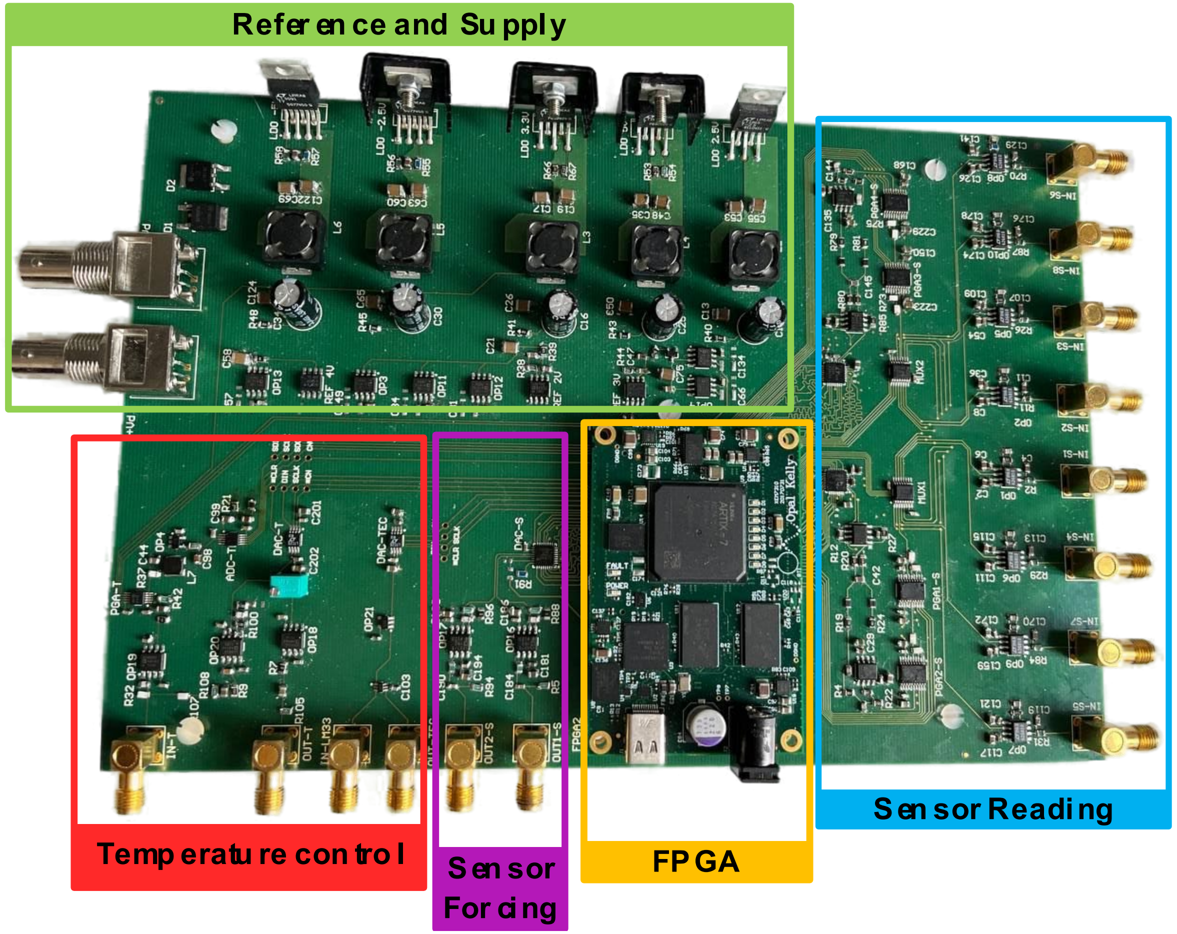






ΔV ∝ number of beads
∝ bio-target

P. Piedimonte et al., Biosensors and Bioelectronics, vol. 221, pp. 113996 (2021)

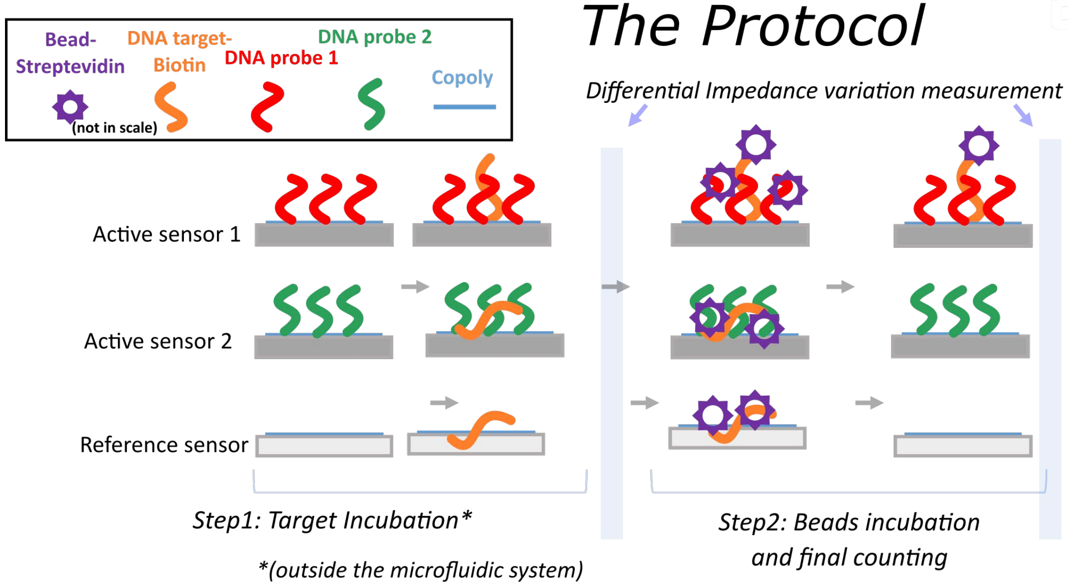


(Dimensions: 18 cm x 22 cm)

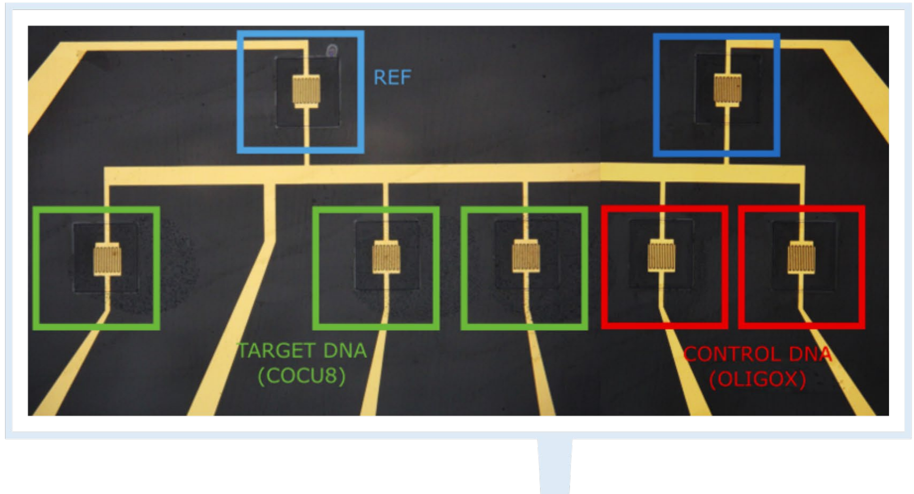
<u>Custom digital lock-in platform:</u>

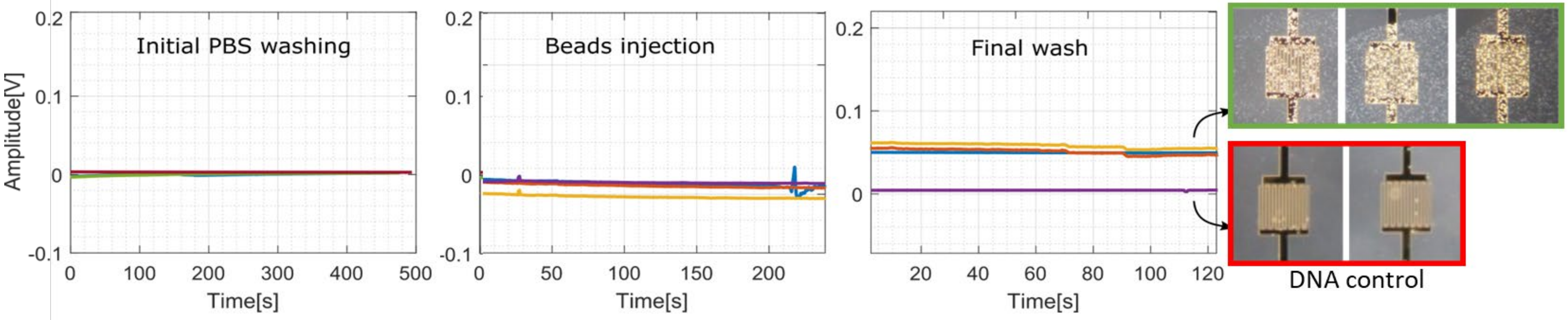
- <u>Compactness and portability</u>
  → Point Of Care configuration
- <u>8 independent channels for multisensing</u>
  → Simultaneous detection of multiple biological targets in a single experiment
- <u>Impedance readout resolution of 100 ppm</u>
  →Digital counting of targets
- <u>Stabilization of the chip temperature with m°C accuracy</u>
  → Stable temperature during the experiment

The Protocol



The DUT



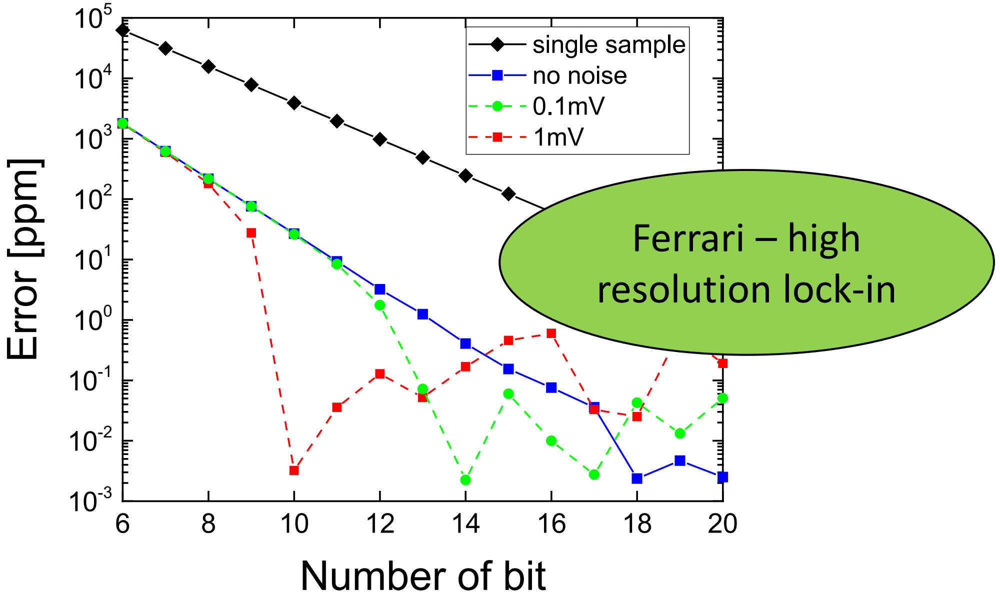


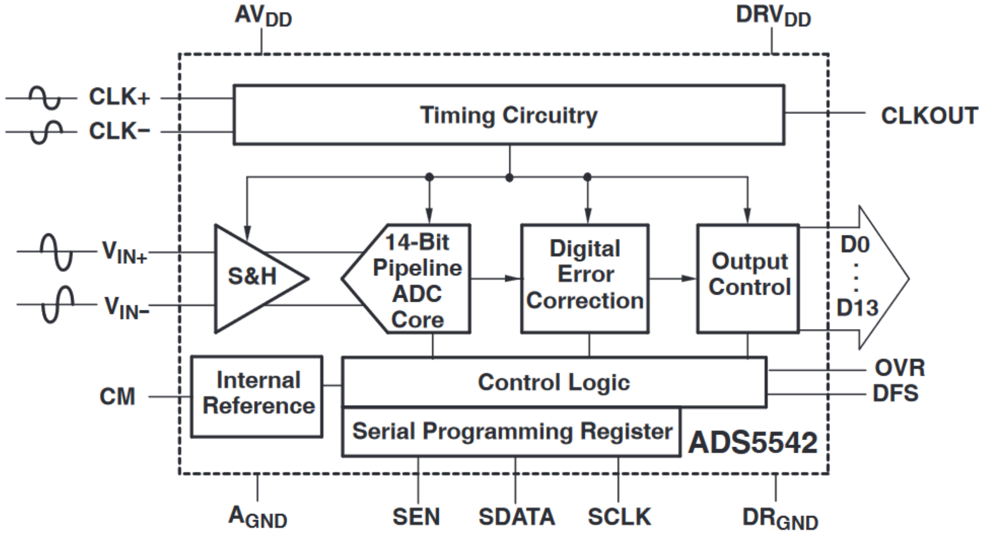
ADC requirements for high-speed (> 1 MHz) digital LIAs

- To meet the resolution and speed requirements of certain applications, ADCs with 12 to 16 bits and up to ~100 MSps are usually required.
- This generates a great amount of data that need to be transmitted to the digital processor (e.g: 80 Msps, 14 bit → 1.12 Gbit/s).
- In order not to require clocks in the GHz range, high-speed ADCs usually have a parallel digital interface at the output.

↓

<u>Digital LIAs with many channels in parallel are hard to be implemented because a huge number of digital lines are needed.</u>





Hybrid lock-in solutions

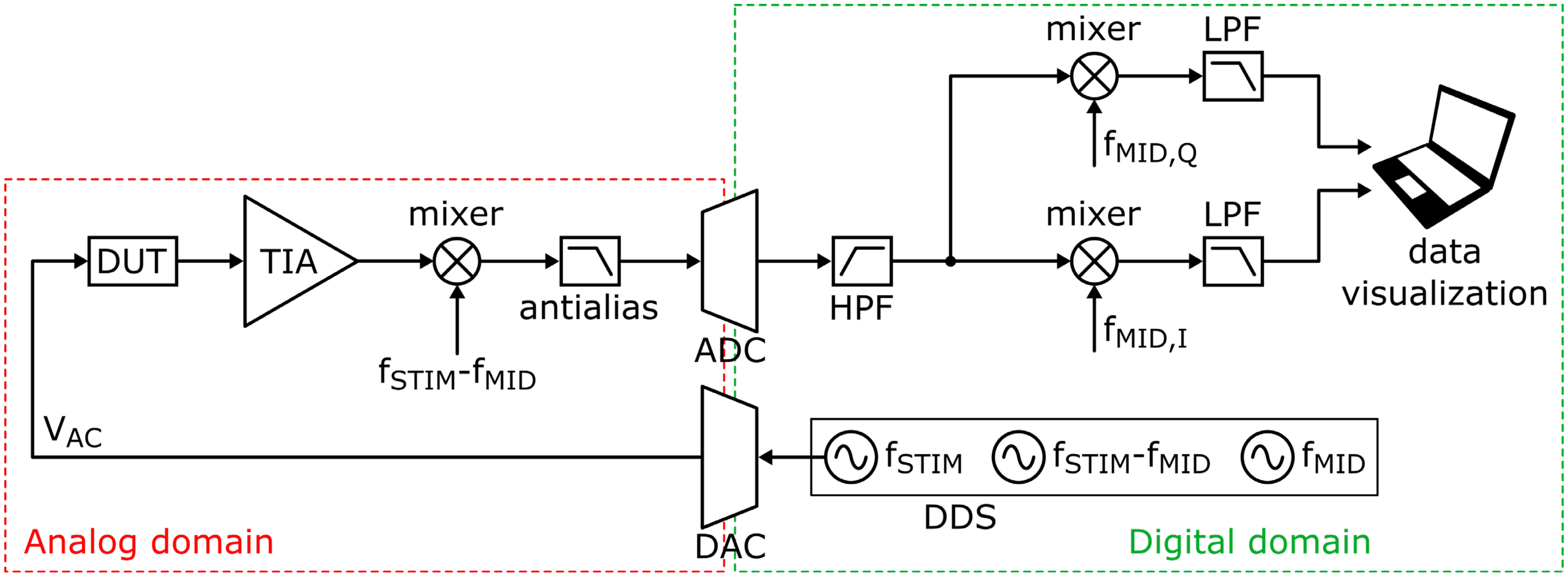
- The design of multichannel high-speed lock-in acquisition systems is challenging because a good compromise between performance, complexity and area occupation needs to be found.
- Digital LIAs offer excellent performance and low area occupation for the front-end circuit, but they require fast ADCs with a good number of bits.
- This introduces a complexity overhead, because a lot of high-speed digital connections need to be managed.
- In addition, digital LIAs cannot be easily operated above ~100 MHz

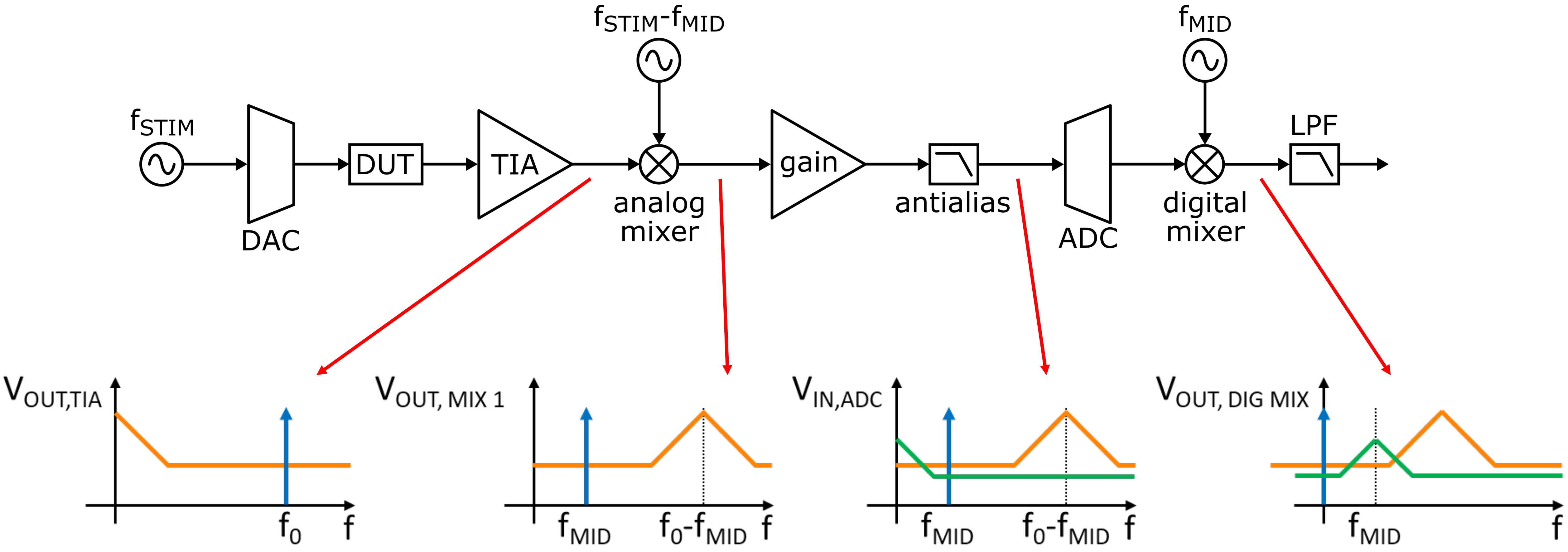
⇩

Is there a way to keep the advantages of digital LIAs while using slow ADCs as in analog implementations?

Heterodyne lock-in detection

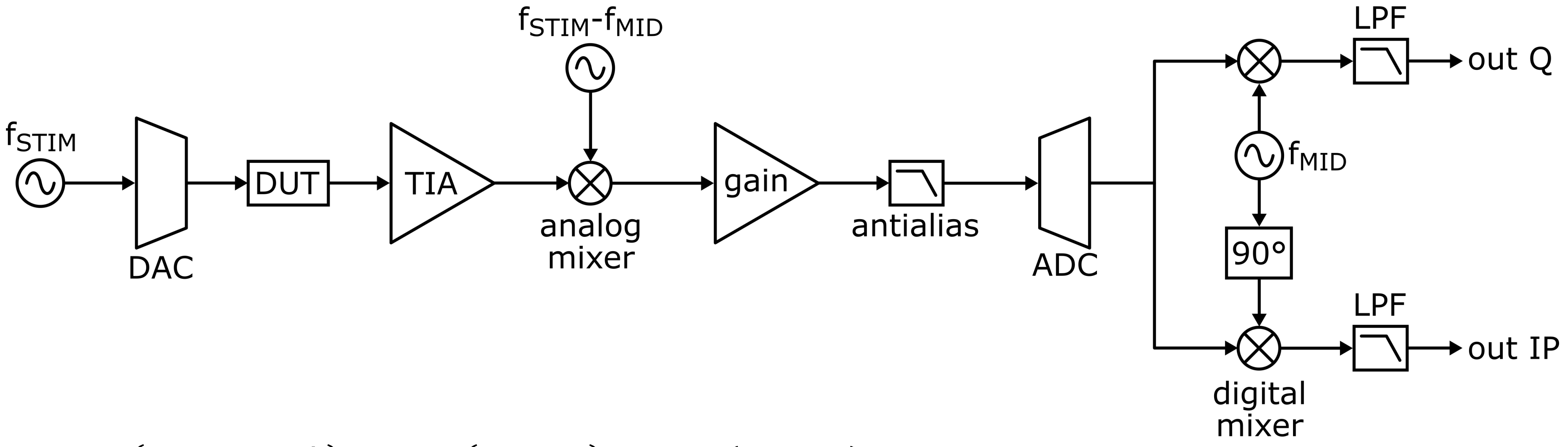
- An analog mixer moves the signal from high frequency to an intermediate frequency.
- The intermediate frequency should be chosen above the 1/f noise corner of the acquisition circuit in order not to degrade the lock-in performance.
- A single slow ADC can be used to digitize the signal at intermediate frequency, without requiring complex handling of high-speed digital signals.
- A second I/Q demodulation is performed digitally to complete the lock-in acquisition.





- The effect of 1/f noise and offset of all stages is canceled!
- <u>Synchronization of the lock-in processing is needed to ensure consistency!!!</u>

Some math



$$V_{OUT,TIA} = A\sin(\omega_{STIM}t + \phi) = B\sin(\omega_{STIM}t) + C\cos(\omega_{STIM}t)$$

$$V_{OUT,\,MIX\,1} = [B\sin(\omega_{STIM}t) + C\cos(\omega_{STIM}t)] \cdot \sin[(\omega_{STIM} - \omega_{MID})t] = \frac{B}{2}\cos(\omega_{MID}t) - \frac{C}{2}\sin(\omega_{MID}t)$$

$$V_{OUT,\,MIX\,2,\,IP} = \left[\frac{B}{2}\cos(\omega_{MID}t) - \frac{C}{2}\sin(\omega_{MID}t)\right]\cos(\omega_{MID}t) = \frac{B}{4}\cos(0) - \frac{C}{4}\sin(0) = \frac{B}{4}$$

$$V_{OUT,\,MIX\,2,\,Q} = \left[\frac{B}{2}\cos(\omega_{MID}t) - \frac{C}{2}\sin(\omega_{MID}t)\right][-\sin(\omega_{MID}t)] = -\frac{B}{4}\sin(0) + \frac{C}{4}\cos(0) = \frac{C}{4}$$

Neglecting high-order harmonics that are filtered

Lock-in synchronization: DDS

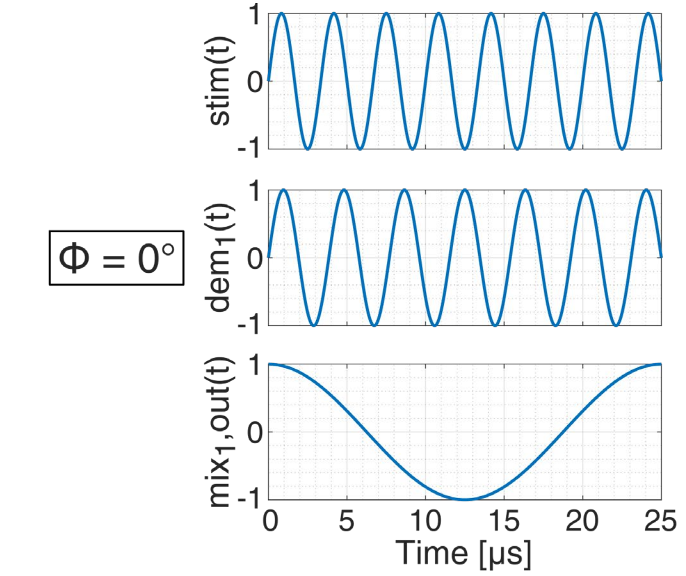
<u>To ensure consistency of the lock-in processing among different experiments:</u>

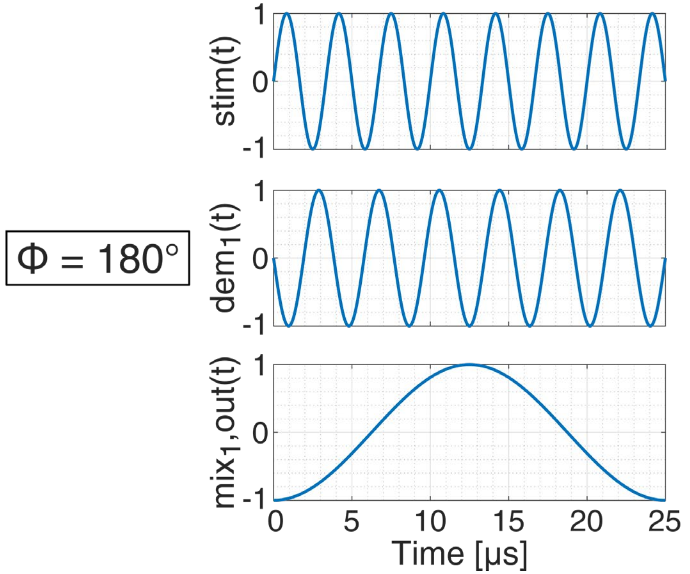
- Use the same clock to drive all the DDSs.
- Compute the frequency word of the intermediate DDS as difference between the other two, to avoid rounding approximations:

$$FW_{STIM} = f_{STIM} \cdot \frac{2^{N_{BIT},DDS}}{f_{CLOCK}} \qquad FW_{MID} = f_{MID} \cdot \frac{2^{N_{BIT},DDS}}{f_{CLOCK}}$$

$$FW_{STIM-MID} = FW_{STIM} - FW_{MID}$$

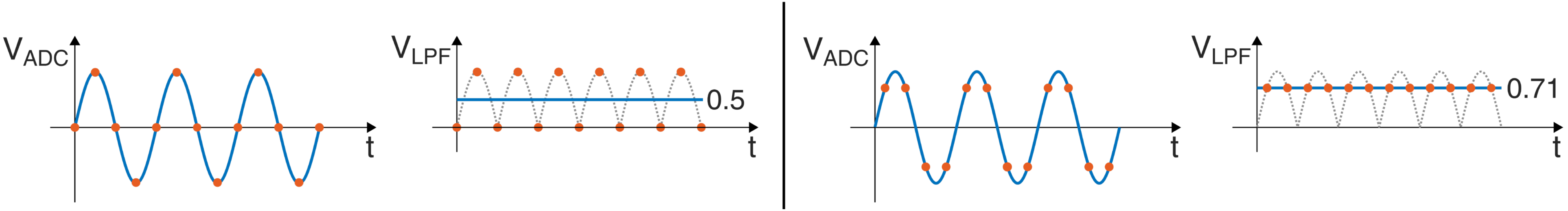
- <u>Always start/stop/update all the DDS simultaneously to keep same initial conditions.</u>





Lock-in synchronization: ADC

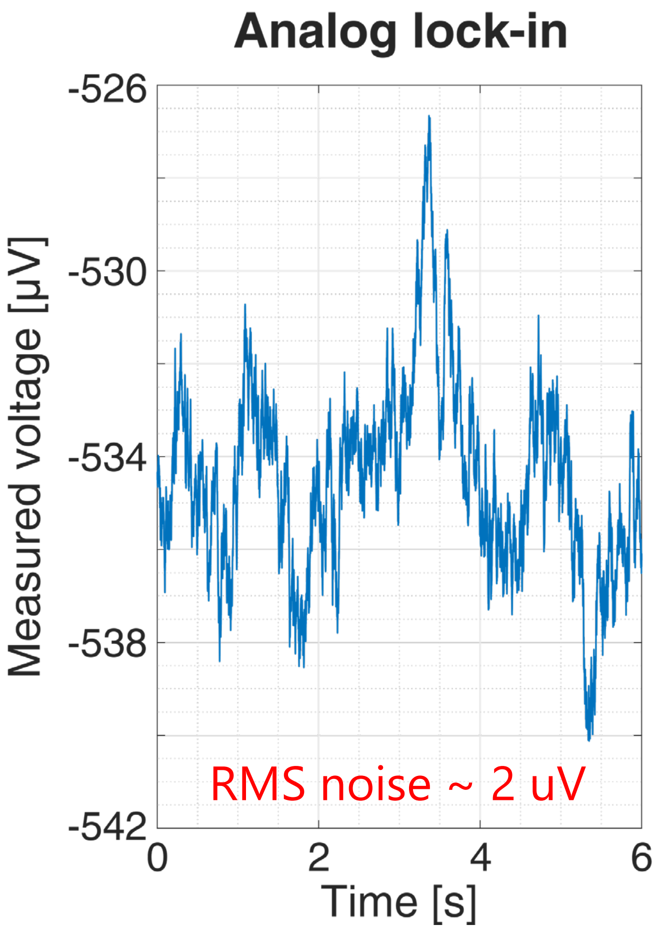
- The synchronization of the ADC conversion is also critical to obtain consistent results among different experiments.
- Sampling the input waveforms in different points results in different demodulation results, because demodulation is a non-linear process.
- The error decreases if the number of samples per period increases, but it can't be completely solved unless proper synchronization is ensured → restart the ADC conversion whenever any parameter of the DDSs are updated to always sample the input waveform in the same points.

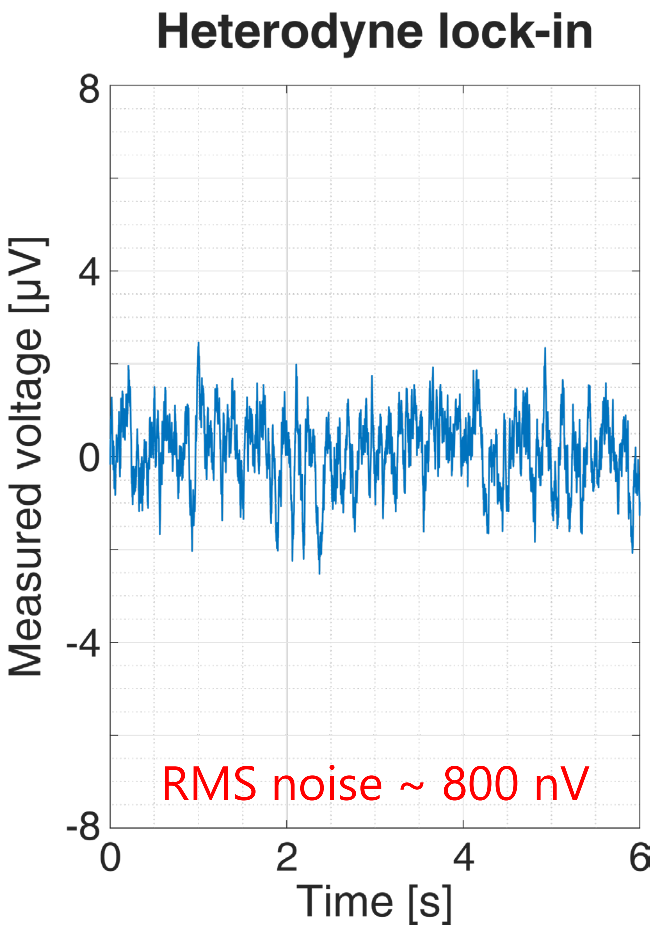


Experimental demonstration of the heterodyne lock-in

- The effect of the acquisition chain offset is removed with the heterodyne technique.
- The readout noise is reduced because the 1/f component is avoided.

- White noise = $200 \mathrm{nV}/\sqrt{\mathrm{Hz}}$
- 1/f noise corner frequency of the acquisition chain = 10 Hz
- Lock-in bandwidth = 10 Hz
- Intermediate frequency = 5 kHz





Conclusions

- Choose the best lock-in architecture depending on the requirements of the application.
- Beware of 1/f noise after analog demodulation to obtain the best performance.
- Carefully design the signal processing chain of digital LIAs.
- Consider hybrid lock-in solutions in those situations where the standard approaches struggle.